82C930

16-Bit Sound Controller

Data Book

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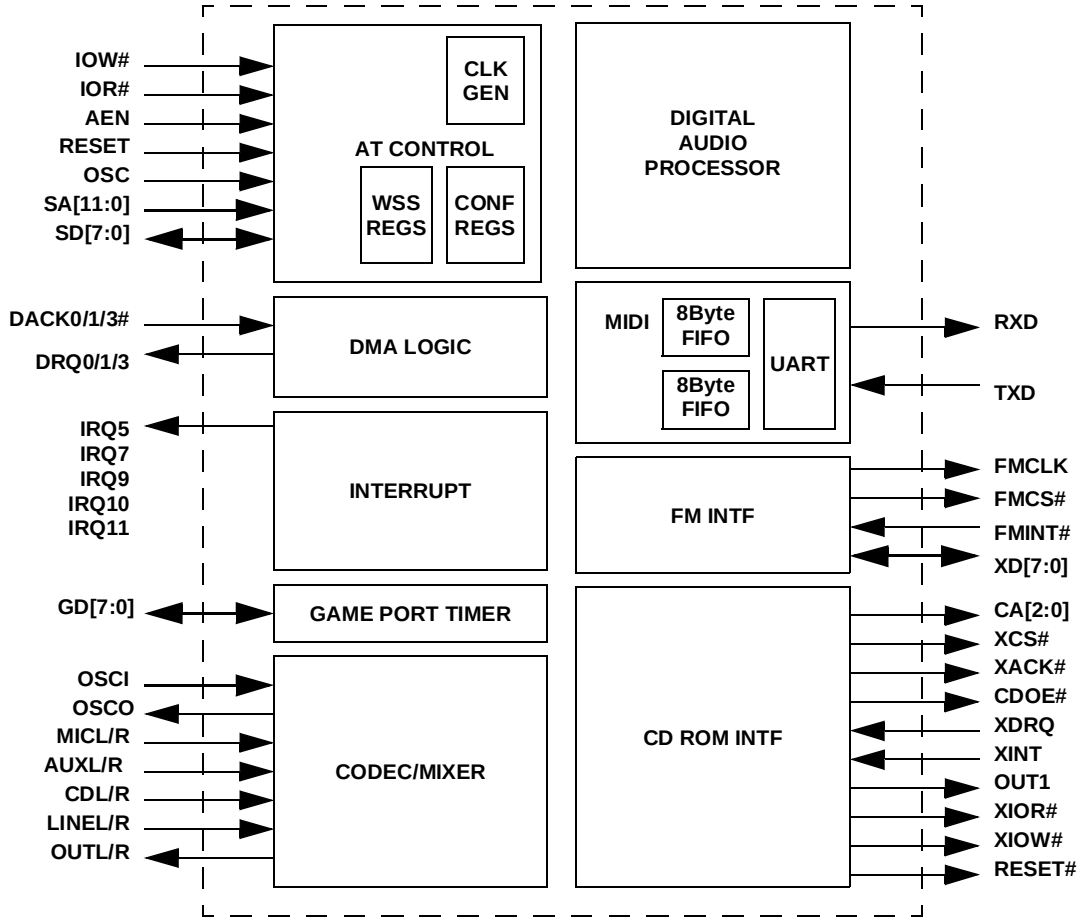
1.0 Overview

The OPTi 82C930 is an integrated sound controller for PC sound applications. 82C930 is compatible with Sound Blaster Pro™, Ad Lib™, MPU-401, and Microsoft Windows Sound System™.

The 82C930 16-bit Sound Controller provides all of the functions and interfaces for the Sound Blaster-compatible and Microsoft Windows Sound System-compatible card. The 82C930 is intended to provide an integrated audio solution for business audio, educational/entertainment sound and multimedia applications.

The 82C930 includes the functions of AT Bus interface, Sound Blaster-compatible Digital Audio Processor, MIDI interface, Windows Sound System interface, FM synthesizer interface, 16-bit Codec/Mixer, Game Port timer, as well as interfaces to four different types of CD ROM's. All DMA and interrupt selections are software programmable. The 82C930 provides enough driving capabilities for all of the interfaces. There is also a power-down mode for power-conscious system designs.

Figure 1-1 Block Diagram



2.0 Features

- Integrated sound controller compatible with
  - Sound Blaster Pro
  - Ad Lib
  - Microsoft Windows Sound System
- Built-in 16-bit Sigma-Delta Stereo Codec
- Built-in 5-channel MPC compatible stereo mixer
- 32-Step master volume control
- 8 or 16-bit sound data up to 48 kHz stereo
- Supports 235 sample rates from 4KHz to 48KHz
- Support IMA ADPCM, u-Law, A-Law decompression
- Integrated MIDI UART with FIFO for both in and out with MPU-401 interface
- Direct OPL2/OPL3/OPL4/... interfaces
- Built-In Game Port Timer
- IDE CD ROM interface
- 20mA drivers for direct AT Bus interface
- Power-down mode
- Silence mode to turn off all audio functions
- All interfaces are software programmable including
  - I/O Address
  - IRQ
  - DRQ
- Dual DMA channels for Full Duplex Operation
- Playback and Capture with On-chip FIFOs for simultaneous playback and record
- MIDI Extension Support
  - Enable MIDI sound generation by OPL4 type of device with an exclusive driver
- 100 pin package

2.1 Applications

Together with the Yamaha OPL3 FM synthesis chip, 82C930 provides the integrated solution for the following applications:

- 16-bit sound quality Sound Blaster + Windows Sound System Compatible Card
- 20 Voice FM Synthesis
- 16-bit CD-quality WAVE audio up to 44.1KHz stereo
- IDE CD ROM interface
- Game Port
- MPU-401 MIDI interface
- OPL4 or other wave table synthesis upgrade

3.0 Signal Description

Figure 3-1 Pin Diagram

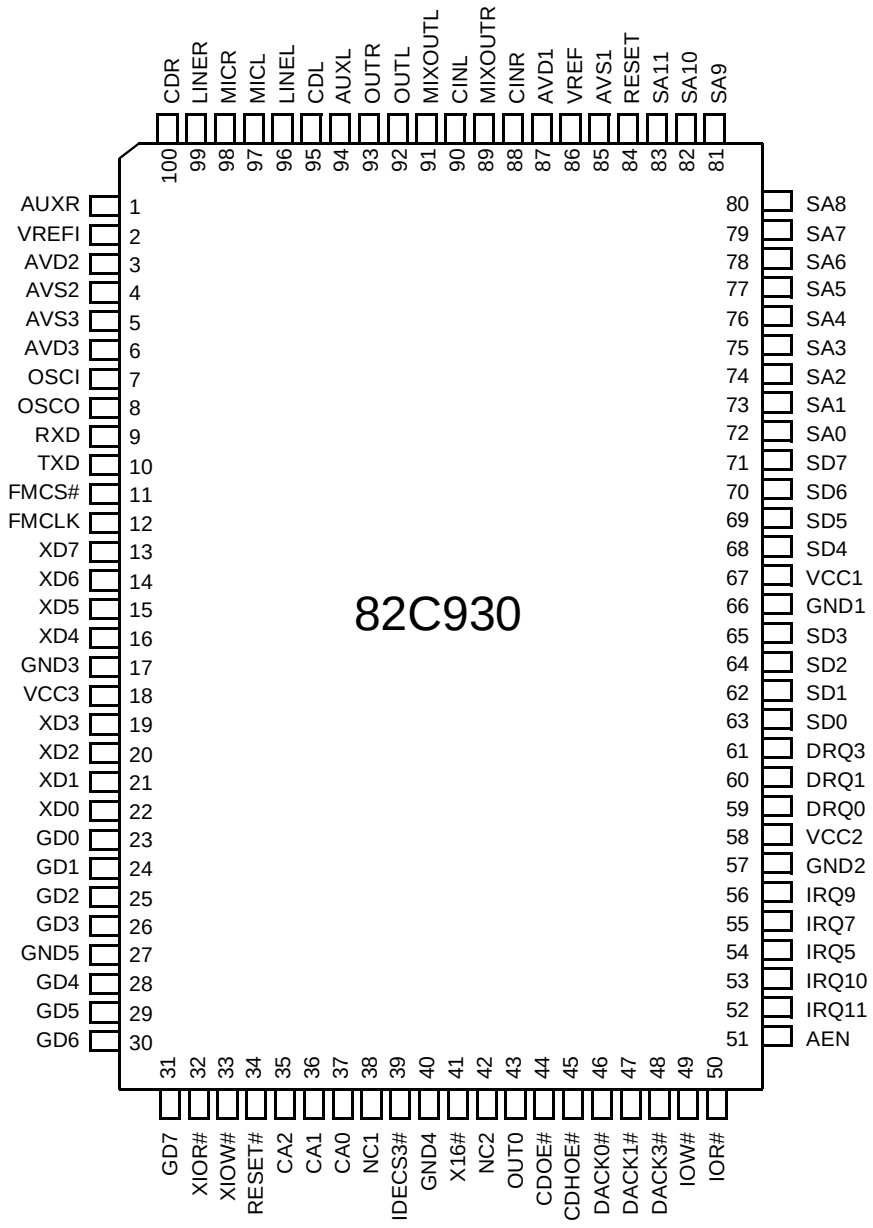


Table 3-1 Numerical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AUXR	26	GD3	51	AEN	76	SA4
2	VREFI	27	GND5	52	IRQ11	77	SA5
3	AVD2	28	GD4	53	IRQ10	78	SA6
4	AVS2	29	GD5	54	IRQ5	79	SA7
5	AVS3	30	GD6	55	IRQ7	80	SA8
6	AVD3	31	GD7	56	IRQ9	81	SA9
7	OSCI	32	XIOR#	57	GND2	82	SA10
8	OSCO	33	XIOW#	58	VCC2	83	SA11
9	RXD	34	RESET#	59	DRQ0	84	RESET
10	TXD	35	CA2	60	DRQ1	85	AVS1
11	FMCS#	36	CA1	61	DRQ3	86	VREF
12	FMCLK	37	CA0	62	SD0	87	AVD1
13	XD7	38	NC1	63	SD1	88	CINR
14	XD6	39	IDECS3#	64	SD2	89	MIXOUTR
15	XD5	40	GND4	65	SD3	90	CINL
16	XD4	41	X16#	66	GND1	91	MIXOUTL
17	GND3	42	NC2	67	VCC1	92	OUTL
18	VCC3	43	OUT0	68	SD4	93	OUTR
19	XD3	44	CDOE#	69	SD5	94	AUXL
20	XD2	45	CDHOE#	70	SD6	95	CDL
21	XD1	46	DACK0#	71	SD7	96	LINEL
22	XD0	47	DACK1#	72	SA0	97	MICL
23	GD0	48	DACK3#	73	SA1	98	MICR
24	GD1	49	IOW#	74	SA2	99	LINER
25	GD2	50	IOR#	75	SA3	100	CDR

Table 3-2 Alphabetical Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
51	AEN	11	FMCS#	98	MICR	62	SD0
94	AUXL	23	GD0	91	MIXOUTL	63	SD1
1	AUXR	24	GD1	89	MIXOUTR	64	SD2
87	AVD1	25	GD2	38	NC1	65	SD3
3	AVD2	26	GD3	42	NC2	68	SD4
6	AVD3	28	GD4	7	OSCI	69	SD5
85	AVS1	29	GD5	8	OSCO	70	SD6
4	AVS2	30	GD6	43	OUT0	71	SD7
5	AVS3	31	GD7	92	OUTL	10	TXD
35	CA2	66	GND1	93	OUTR	67	VCC1
36	CA1	57	GND2	84	RESET	58	VCC2
37	CA0	17	GND3	34	RESET#	18	VCC3
45	CDHOE#	40	GND4	9	RXD	86	VREF
95	CDL	27	GND5	72	SA0	2	VREFI
44	CDOE#	39	IDECS3#	73	SA1	41	X16#
100	CDR	50	IOR#	74	SA2	22	XD0
90	CINL	49	IOW#	75	SA3	21	XD1
88	CINR	54	IRQ5	76	SA4	20	XD2
46	DACK0#	55	IRQ7	77	SA5	19	XD3
47	DACK1#	56	IRQ9	78	SA6	16	XD4
48	DACK3#	53	IRQ10	79	SA7	15	XD5
59	DRQ0	52	IRQ11	80	SA8	14	XD6
60	DRQ1	96	LINEL	81	SA9	13	XD7
61	DRQ3	99	LINER	82	SA10	32	XIOR#
12	FMCLK	97	MICL	83	SA11	33	XIOW#

3.1 Signal Definition

I = Input
O = Output
I/O = Bi-Directional
T = Tri-State
OD = Open-Drain

3.1.1 AT Bus Signal (35)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
IOW#	49	I	TTL-Smt 50KΩ pull-up	IO Write Command	AT BUS
IOR#	50	I	TTL-Smt 50KΩ pull-up	IO Read Command	AT BUS
AEN	51	I	TTL-Smt	DMA Address Enable	AT BUS
RESET	84	I	TTL-Smt 50KΩ pull-down	System Reset Input	AT BUS
SA[11:0]	83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73, 72	I	TTL	System Address	AT BUS
SD[7:0]	71, 70, 69, 68, 65, 64, 63, 62	I/O	TTL/20mA	System Data Bus	AT BUS
DACK0/1/3#	46, 47, 48	I	TTL 50KΩ pull-up	DMA Acknowledge	AT BUS
DRQ0 DRQ1 DRQ3	59 60 61	T	16mA 50KΩ pull-down	8-bit DMA Request	AT BUS
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	54 55 56 53 52	OD I/O	16mA 50KΩ pull-up TTL	Interrupt Request IRQ7-11 bidirectional for WSS auto interrupt determination	AT BUS

3.1.2 MIDI Interface Signal (2)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
RXD	9	I	TTL-Smt	Receive Data	MIDI Port
TXD	10	O	20mA	Transmit Data	MIDI Port

3.1.3 FM Interface Signal (10)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
FMCLK YA2	12	O	8mA	FM Clock output high during power-down/ OPL4 Address[2]	FM
FMCS#	11	O	8mA	FM Chip Select, Asserted for IO address SBBase + 0-3 SBBase + 8-9 388-38B	FM
XD[7:0]	13-16, 19-22	I/O	TTL / 8mA 50KΩ pull-up	Local Data Bus Internal test node status in Digital test mode.	FM

3.1.4 CD ROM Interface Signal (13)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
CA1	36	O	12mA	IDE: CA1	CD ROM
CA0	37	O	12mA	IDE: CA0	CD ROM
NC1	38	O	12mA	No connect	NC
IDECS3#	39	O	12mA TTL	IDE: CS3X#	CD ROM
X16#	41	I	TTL 50KΩ pull-down	IDE: 16-bit IO	CD ROM
NC2	42	I	TTL 50KΩ pull-up	No connect	NC
CA2/ OUT1	35	O	TTL 12mA	IDE: CA2 Others: OUT1	CD ROM
OUT0/ CMD#	43	O	12mA		CD ROM
CDOE#	44	O	8mA	CD data buffer output enable	
CDHOE#	45	O	8mA	IDE: [15:8] data buffer output enable	
XIOR#	32	O	12mA	Buffered IOR#	CD ROM, FM
XIOW#	33	O	12mA	Buffered IOW#	CD ROM, FM
RESET#	34	O	12mA	Buffered RESET, active low	CD ROM, FM

3.1.5 Game Interface Signal (8)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
GD[7:4]	31-28	I	CMOS-Smt 50KΩ pull-up	Game Port Data	
GD[3:0]	26-23	I/O	CMOS-Smt 13.5mA		

3.1.6 Codec/Mixer Signal (18)

Pin Name	Pin #	I/O	I/O Type	Function	To/From
MICL/R	97, 98	I	Analog	MIC input Left/Right	
LINEL/R	96, 99	I	Analog	LINE input Left/Right	
CDL/R	95, 100	I	Analog	CD input Left/Right	
AUXL/R	94, 1	I	Analog	AUX input Left/Right	
OUTL/R	92, 93	O	Analog 10KΩ, 25pF drive	Output Left/Right	
MIXOUTL/R	91, 89	O	Analog	Mixer output	
CINL/R	90, 88	I	Analog	ADC Filter Pins	
VREFI	2	O	Analog	Analog common. Normally connected to AVS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.	
VREF	86	O	Analog	Voltage reference. Nominal 2.5V reference available externally. Not meant for current sourcing or sinking. Normally connected to AVS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.	
OSCI	7	O	Analog	Oscillator input. A 14.318MHz crystal oscillator is to be connected across the pin and the OSCO pin.	
OSCO	8	O	Analog	Oscillator output. See OSCI.	

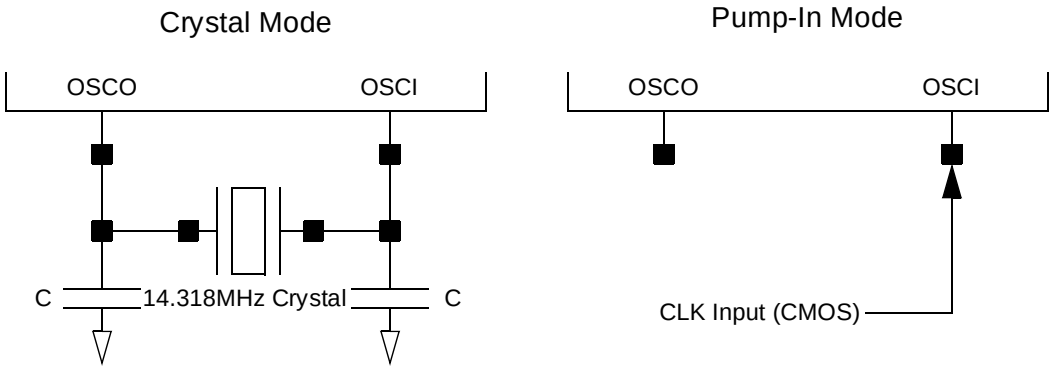
3.1.7 Power Pins (14)

Pin Name	Pin #
V_{CC}	18,58,67
GND	17,27,40,57,66
AV_{DD}	3,6,87
AV_{SS}	4,5,85

3.1.8 External Components

Pin Name	External Components
OSCI	14.318MHz CRYSTAL
OSCO	14.318MHz CRYSTAL

Figure 3-2 External Components



* C is a 22pF capacitor
* Crystal Oscillator powered down when PDN asserted

4.0 Register Description

The 82C930 uses the base addresses shown in Table 4-1.

Table 4-1 82C930 I/O Base Addresses

Function	Base	Address Selections
Configuration Registers	MCBase	F8F; E0E,F/FFE,F
Digital Audio Processor	DABase	220/240
Windows Sound System	WSBase	530/640/E80/F40
Proprietary CD ROM	CDBase	320/330/340/360
IDE CD ROM	IDEBase	170 & 370
AdLib	ALBase	388
OPL4	OPL4Base	380
MPU-401	MIDIBase	300/310/320/330

Table 4-2 82C930 Register Map

I/O Address	Description	R/W
SBBase + 0 ALBase + 0	Left FM Status Port	R only
SBBase + 0 ALBase + 0	Left FM Register Address Port	W only
SBBase + 1 ALBase + 1	Left FM Data Port	W only
SBBase + 2 ALBase + 2	Right FM Register Address Port	W only
SBBase + 3 ALBase + 3	Right FM Data Port	W only
SBBase + 4	Mixer Address Port	W only
SBBase + 5	Mixer Data Port	R/W
SBBase + 6	Digital Audio Processor Software Reset	W only
SBBase + 8	FM Status Port	R only
SBBase + 8	FM Register Address Port	W only
SBBase + 9	FM Data Port	W only
SBBase + A	Digital Audio Processor Read Data	R only, Digital Audio Processor AO = 0
SBBase + C	Digital Audio Processor Write Data/ Cmd	W only, Digital Audio Processor AO = 1
SBBase + C	Digital Audio Processor Write Buffer Status	R only, Digital Audio Processor AO = 1
SBBase + E	Digital Audio Processor Output Buffer Status Reg	R only, Digital Audio Processor AO = 1
WSBase + 0-3	Configuration	W only

I/O Address	Description	R/W
WSBase + 0-3	Version	R only
WSBase + 4	Codec Index Reg	R/W, exists in Codec and shadowed in 82C930
WSBase + 5	Codec Indexed Data Reg	R/W, exists in Codec only
WSBase + 6	Codec Status Reg	R/W, exists in Codec only
WSBase + 7	Codec Direct Data	R/W, exists in Codec only
200-201	Game Port	R/W
CDBase + 0-3	CD ROM Reg	R/W
F8F	Password Register/MCBase	W only
MCBase+1	MC1	R/W
MCBase+2	MC2	R/W
MCBase+3	MC3	R/W
MCBase+4	MC4	R/W
MCBase+5	MC5	R/W
MCBase+6	MC6	R/W
MCBase+7	MC7	R/W
MCBase+8	MC8	R/W
MCBase+9	MC9	R/W
MCBase+10	MC10	R/W
MCBase+11	MC11	R/W
MCBase+12	MC12	R/W
380-383/388-38B	OPL4	R/W
388-38F	OPL5	R/W

4.1 82C930 Register Definition

Note (1) All Registers are set to '0' after reset.
(2) The default software setting is highlighted with **BOLD** characters.

4.1.1 Direct MC Register

MCBase Write Only Port = F8F							
7	6	5	4	3	2	1	0
PassWD = **E4**							
PASS EN#			MCA4	MCA3	MCA2	MCA1	MCAD0

MCBase is the indirect MC address register that controls the access of other MC registers. To access MC1 to MC12. MCBase must be written with the index address first. This register is always protected by the password. Pass Word is “E4”.

Pass En#: Pass word protection enable control for the MC registers. '0' enables protection.

MCIdx Port Address = b"111[MCA4] - [MCA3:0] - 1110"							
7	6	5	4	3	2	1	0
Index							

MCData Port Address = b" 111[MCAD4] - [MCA3:0] - 1111"							
7	6	5	4	3	2	1	0
Data							

4.1.2 Indirect MC Registers

MC1 Base/Type configuration Register							
7	6	5	4	3	2	1	0
SB BASE		WSS BASE[1:0]		CDTYPE[2:0]			GPEN#
SB Base Address 0 = 220 1 = 240		WSS Base Address: 00 = WSBase = 530 01 = WSBase = E80 10 = WSBase = F40 11 = WSBase = 604		000 = CD is disabled 001 = reserved 010 = reserved 011 = reserved 100 = Secondary IDE 101 = Primary IDE 110 = reserved 111 = reserved			Game Port Enable 0 = enabled 1 = disabled

SB Base: SB I/O Base Address.

Sound Base: Wss I/O Base Address. MC[5:4] selects the I/O base address among the four specified addresses.

CD Type: Type of CD ROM Interface
This field selects one of the three CD ROM interfaces supported by 82C930.

Game Port Enable:

MC2 CD Configuration Register							
7	6	5	4	3	2	1	0
CDSEL[1:0]		IDE DEN	Reserved				
CD Base Address Select 00 = CDBase = 340 01 = CDBase = 330 10 = CDBase = 360 11 = CDBase = 320		IDE DMA enable 0 = disable 1 = enable					

CDSEL: CD ROM Base Address
The Base I/O address for CD ROM interface.

CDIRQ: CD ROM Interrupt Select
This field selects the interrupt channel for CD ROM interface. When users change IRQ selection through software, false IRQ's will be generated due to the open-drain drivers employed on the IRQ outputs. During this time, interrupt needs to be disabled temporarily.

CDDRQ: CD ROM DMA Select

MC3 SB/WSS Configuration Register							
7	6	5	4	3	2	1	0
CNFG7	ISS	SBISEL[2:0]			SBDSEL[2:0]		
Reserved Must be '0'	Reserved Must be '0' for normal operation in WSS	DAP IRQ SELECT: 000 = IRQ Disable 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			DAP DMA SELECT: 000 = Disable 001 = DRQ0 010 = DRQ1 011 = DRQ3 100 = Disable DRQ1 * 101 = DRQ0 DRQ1 * 110 = DRQ1 DRQ0 * 111 = DRQ3 DRQ0 *		

*. These should be the DMA channel selection when running MEC operation in DMA mode. SDC should be set to '0'.

MC4 User Programmable General Purpose Register							
7	6	5	4	3	2	1	0
FCC[1:0]		OPL[1:0]		DACZ	SILENCE	SBVER	
Playback FIFO: 00 = Empty 01 = Full-2 10 = Full-4 11 = Not Full		OPL Select: 00 = OPL2 01 = OPL3 10 = OPL4 11 = OPL5		DAC Zero: 0 = Hold 1 = Clear	0 = Audio 1 = Clear	00 = 2.1 01 = 1.5 10 = 3.2 11 = 4.4	

GPOUT[1:0]: General Purpose Outputs

OPL[1:0]: Yamaha Synthesis Chip type selection

SILENCE: Disable host access to FM, SB/WSS

SBVER: Sound Blaster version.

MC5 Option Register							
7	6	5	4	3	2	1	0
Reserved		MODE2	ADPCM EN	CFIFO	EP EN	Reserved	Reserved
PEN RST Enable: **0 = Disable** **Must be 0**		CS4231: 0 = Mode 1 **1 = Mode 2**	ADPCM Enable: 0 = Disable **1 = Enable**	C-FIFO Enable: 0 = Disable **1 = Enable**	EP Enable: 0 = Enable **1 = Disable**	DRQ TM Enable: **0 = Disable** **Must be 0**	FSMUTE Enable: **0 = Disable** **Must be '0'**

MODE2: To enable Codec's Extended Mode (mode2).

ADPCMEN: To enable SB ADPCM.

CFIFO: To enable command FIFO in Sound Blaster mode.

EPEN: To enable Volume Effect for Sound Blaster Pro mixer voice volume emulation.

MC6 MIDI Interface Register (write only)							
7	6	5	4	3	2	1	0
MPU401 EN	MPU401 Base		MPU401 Interrupt		CDOE SEL	WSS EN	SB EN
0 = disable 1 = Enable	00 = MPUBase = 330 01 = MPUBase = 320 10 = MPUBase = 310 11 = MPUBase = 300		00 = IRQ9 01 = IRQ10 10 = IRQ5 11 = IRQ7		**0 = Use CMD** 1 = Do not use CMD	0 = Disable **1 = Enable**	0 = disable **1 = enable**

MC7 Semaphore Register (Software use only)							
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

MC8 MIDI Extender Control Register							
7	6	5	4	3	2	1	0
MEC RDY	MEC EMPTY	MEC INT.	MEC ISEL[1:0]		MEC DMAEN	MEC IEN	MEC EN
MEC FIFO Ready	MEC FIFO Empty	MEC Int Status	MEC Interrupt Select 00 = INT5 01 = INT7 10 = INT10 11 = INT11		MEC DMA Enable 0 = Disable 1 = Enable	MEC Int. Enable 0 = Disable 1 = Enable	MEC Enable 0 = Disable 1 = Enable

MECINT: MEC Interrupt Status. In PIO mode, this bit is automatically cleared when the FIFO is empty. In DMA mode, a write to MC8 clears the MCEINT bit.

MC9 Reserved							
7	6	5	4	3	2	1	0
Reserved							

MC10 Reserved							
7	6	5	4	3	2	1	0
Reserved							

MC11 Status Register							
7	6	5	4	3	2	1	0
PDRQ	CDRQ	MPUI	CDI	CI	PI	PE	
Playback DMA	Capture DMA	MPU Interrupt	CD Interrupt	Capture Interrupt	Playback Interrupt	Playback End	

MC12 Reserved							
7	6	5	4	3	2	1	0
Reserved							

4.1.3 DAP Registers

Digital Audio Processor Reset (SBBase+C)							
7	6	5	4	3	2	1	0
"Don't care"							RESET

RESET = '1' will perform a software reset on the Digital Audio Processor at the end of the IO write command. It actually sets a software reset flag. This software reset is terminated by performing another write at this location with RESET = '0'. A system reset will reset the software reset flag and thus terminates the software reset.

Digital Audio Processor Read Data (SBBase+A) Read Only							
7	6	5	4	3	2	1	0
DATA							

This is the data output port of the Digital Audio Processor.

Digital Audio Processor Write Buffer Status (SBBase+C) Read Format							
7	6	5	4	3	2	1	0
IBFULL	(SBBase+A)[6:0]						

IBFULL is '1' when the Digital Audio Processor Input Buffer is full. This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal Digital Audio Processor.

Digital Audio Processor Data/Command Register (SBBase+C) Write Format							
7	6	5	4	3	2	1	0
Command/Data							

This is the data/command write port for the Digital Audio Processor.

Digital Audio Processor Output Buffer Status (SBBase+E) Read Only							
7	6	5	4	3	2	1	0
OBFULL	Output Buffer [6:0]						

OBFULL = 1 when the Digital Audio Processor Output Buffer is full. This flag is set in the Digital Audio Processor when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.

Reading this register will also clear the Digital Audio Processor interrupt request.

4.1.4 WSS Registers

WSS Configuration Register (WSBase+0-3) Write Only							
7	6	5	4	3	2	1	0
Reserved	ISS	WSIRQ			WSDRQ		
	0 = normal 1 = auto interrupt selection	000 = disabled 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			Playback Capture 000 = disabled disabled 001 = DRQ0 disabled 010 = DRQ1 disabled 011 = DRQ3 disabled 100 = Disabled DRQ1 101 = DRQ0 DRQ1 110 = DRQ1 DRQ0 111 = DRQ3 DRQ0		

ISS: IRQ Sense Source

WSS Version Register (WSBase+0-3) Read Only							
7	6	5	4	3	2	1	0
Channel Available	IrqSense	Version					
0 = DRQ0/1/3 and IRQ7/9/10/11 available 1 = DRQ1/3 and IRQ7/9 available	0 = no interrupt 1 = WSS interrupt active	04h					

4.1.5 AD1848 Emulation Register

4.1.5.1 Direct Registers

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0
R1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R2	1	0	CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT
R3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

4.1.5.2 Indirect Registers

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	-	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	-	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8	FM1	FM0	C/L	S/M	CSF2	CSF1	CSF0	C2SL
9	CPIO	PPIO	-	-	ACAL	SDC(1)	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN(2)	-
11	COR	PUR	ACI	DRS	OOR1	OOR0	ORL1	ORL0
12	0	MODE2	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
18	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
20	LMM	-	-	-	LMG3	LMG2	LMG1	LMG0
21	RMM	-	-	-	RMG3	RMG2	RMG1	RMG0
22	LOM	-	-	LOG4	LOG3	LOG2	LOG1	LOG0

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
23	ROM	-	-	ROG4	ROG3	ROG2	ROG1	ROG0
24	IMA REF							
28	FMT1	FMT0	C/L	S/M				
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

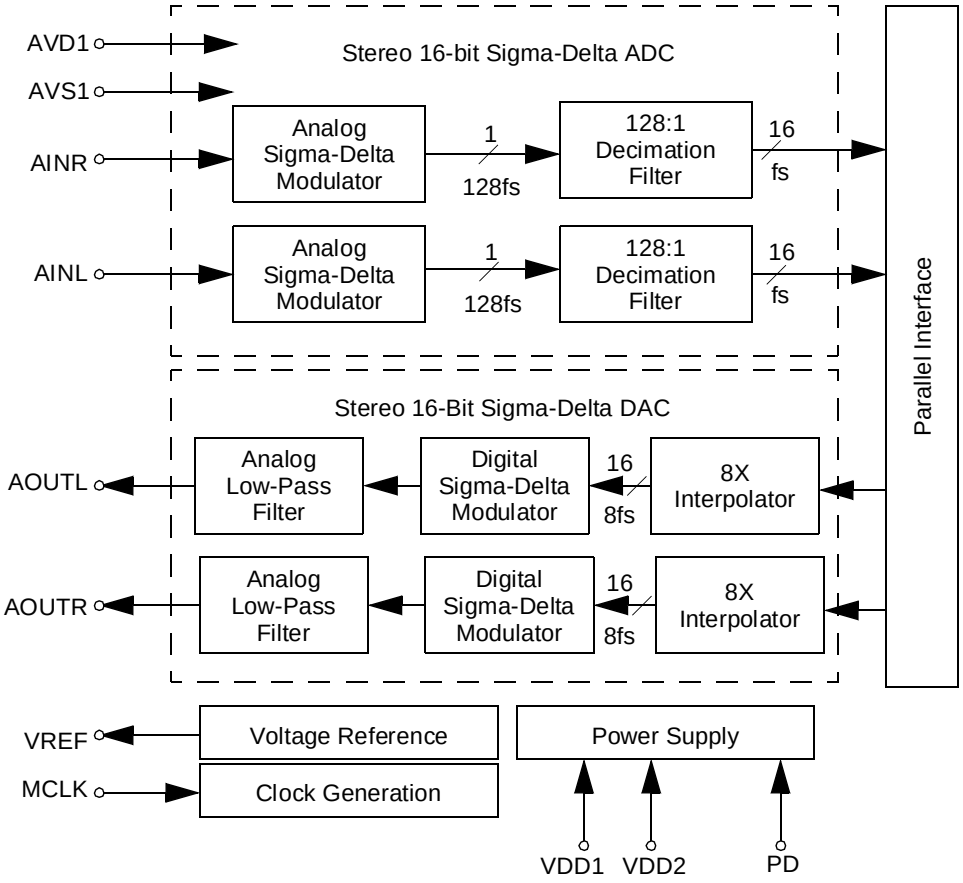
Note 1.SDC: In SB mode, SDC is set when playback or capture DMA started, reset when DMA end.
2.IEN: In SB mode, software driver should set IEN to '1'.
3.SB/WSS mode switch: In SB mode, software driver should set CDF to 8 bit PCM mode (R8: FM1,FM-,C_L).

5.0 16-Bit Stereo Sigma-Delta CODEC

5.1 Features

- Sigma-Delta Stereo ADC with 128X Over-sampling
- Sigma-Delta Stereo DAC with 128X Over-sampling
- On-Chip 8X Interpolation Filter
- On-Chip Analog Post Filter
- Single-Ended Input and Output
- Sampling Rate of 5KHz to 48KHz

Figure 5-1 Functional Block Diagram



5.2 Overview

The CODEC parallel interface provides a means to read and write 16-bit stereo data from the ADC or to the DAC respectively. The interface consists of the following lines:

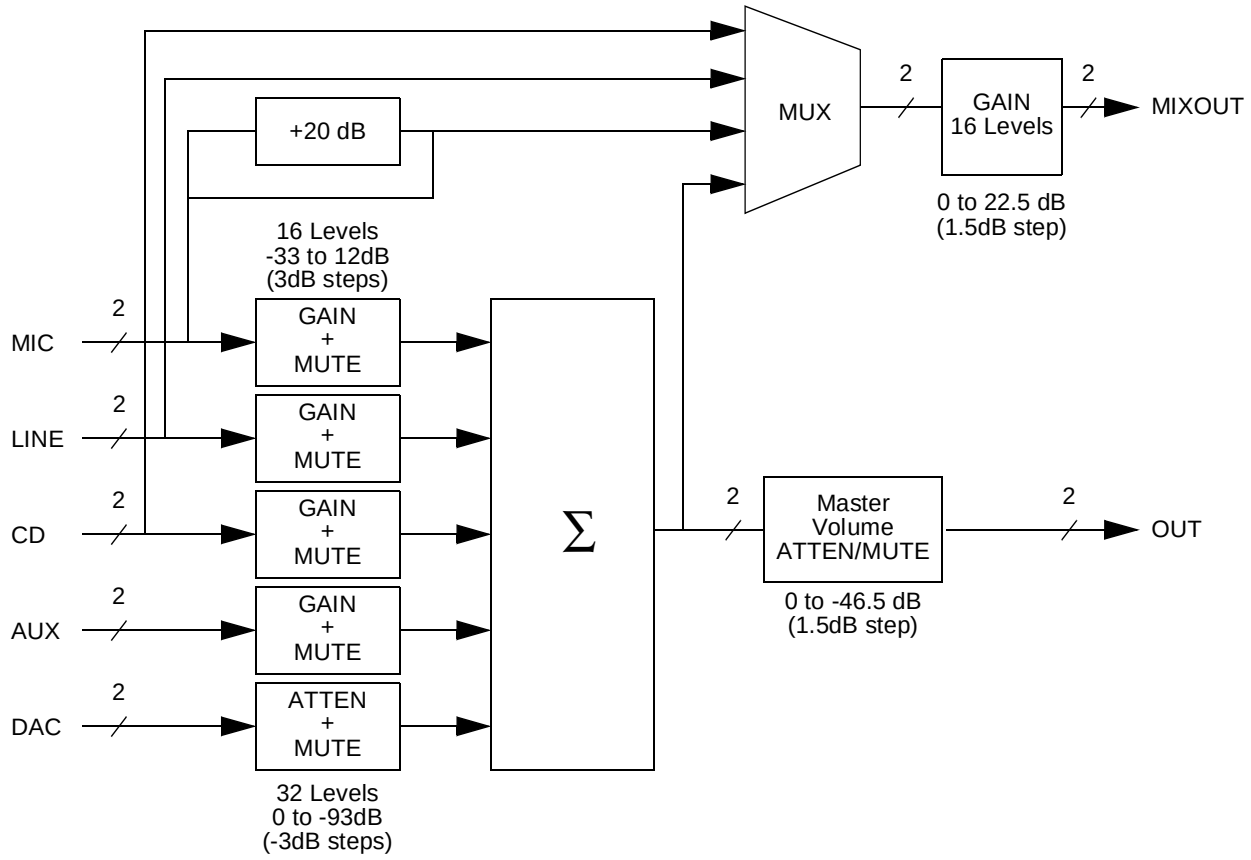
- DAC[15:0] - to write to the DAC 16-bit input
- ADC[15:0] - to read the ADC 16-bit output
- L/R - to select between the Left and Right channels for both the ADC and DAC data.

The DAC Left/Right 16-bit input data are multiplexed onto DAC[15:0] and fed into the CODEC. The L/R signal qualifies the data. The period of L/R is equal to that of the CODEC sampling frequency. One set of Left/Right 16-bit input data to the DAC is sent every L/R cycle. When L/R is low, the data on DAC[15:0] is meant for the left channel; when L/R is high, the data is meant for the right channel. This means that the DAC treats data packets L1 and R1 as belonging to the same sampling instance; while L2 and R2 are data for the next sampling instance.

The ADC Left/Right 16-bit output data are similarly multiplexed onto the ADC[15:0] bus.

6.0 Mixer

Figure 6-1 Mixer Block Diagram



6.1 Mixer Register Descriptions

Table 6-1 Mixer Register Map

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0	MIXOUT Left	SS1	SS0	MGE	--	G3	G2	G1	G0
1	MIXOUT Right	SS1	SS0	MGE	--	G3	G2	G1	G0
2	CD Left	MT	--	--	G3	G2	G1	G0	--
3	CD Right	MT	--	--	G3	G2	G1	G0	--
4	AUX Left	MT	--	--	G3	G2	G1	G0	--
5	AUX Right	MT	--	--	G3	G2	G1	G0	--
6	DAC Left	MT	--	G4	G3	G2	G1	G0	--
7	DAC Right	MT	--	G4	G3	G2	G1	G0	--
18	LINE Left	MT	--	--	G3	G2	G1	G0	--

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
19	LINE Right	MT	--	--	G3	G2	G1	G0	--
20	MIC Left	MT	--	--	--	G3	G2	G1	G0
21	MIC Right	MT	--	--	--	G3	G2	G1	G0
22	OUT Left	MT	--	--	G4	G3	G2	G1	G0
23	OUT Right	MT	--	--	G4	G3	G2	G1	G0

Note SS1-SS0 Source Select
0 = LINE
1 = CD
2 = MIC
3 = MIXER

MT Mute Enable

MGE MIC +20dB Gain Enable

G3-G0 Gain Select - 16 levels of gain control from
0dB to 22.5dB in 1.5dB steps for MIXOUT outputs.
-33dB to 12dB in 3.0db steps for MIC, LINE, CD, and AUX inputs.

G4-G0 Gain Select - 32 levels of gain control from
-46.5dB to 0dB in 1.5dB steps for OUT outputs.
-93dB to 0dB in 3.0dB steps for DAC inputs.

6.2 Default Mixer Register Values

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
0	MIXOUT Left	0	0	0	--	0	0	0	0
1	MIXOUT Right	0	0	0	--	0	0	0	0
2	CD Left	1	--	--	0	1	0	0	--
3	CD Right	1	--	--	0	1	0	0	--
4	AUX Left	1	--	--	0	1	0	0	--
5	AUX Right	1	--	--	0	1	0	0	--
6	DAC Left	1	--	0	0	0	0	0	--
7	DAC Right	1	--	0	0	0	0	0	--
18	LINE Left	1	--	--	0	1	0	0	--
19	LINE Right	1	--	--	0	1	0	0	--
20	MIC Left	1	--	--	--	0	1	0	0
21	MIC Right	1	--	--	--	0	1	0	0
22	OUT Left	1	--	--	0	0	1	0	0
23	OUT Right	1	--	--	0	0	1	0	0

Note These default values are loaded only upon the assertion of the RESET signal.

6.3 Mixer Gain Setting

6.3.1 MIC, LINE, CD, UAX Registers

G3	G2	G1	G0	Gain (dB)
0	0	0	0	+12
0	0	0	1	+9
0	0	1	0	+6
0	0	1	1	+3
0	1	0	0	0
0	1	0	1	-3
0	1	1	0	-6
0	1	1	1	-9
1	0	0	0	-12
1	0	0	1	-15
1	0	1	0	-18
1	0	1	1	-21
1	1	0	0	-24
1	1	0	1	-27
1	1	1	0	-30
1	1	1	1	-33

6.3.2 MIXOUT Register

G3	G2	G1	G0	Gain (dB)
0	0	0	0	0
0	0	0	1	+1.5
0	0	1	0	+3
0	0	1	1	+4.5
0	1	0	0	+6
0	1	0	1	+7.5
0	1	1	0	+9
0	1	1	1	+10.5
1	0	0	0	+12
1	0	0	1	+13.5
1	0	1	0	+15
1	0	1	1	+16.5
1	1	0	0	+18
1	1	0	1	+19.5
1	1	1	0	+21
1	1	1	1	+22.5

6.3.3 OUT Register

G4	G3	G2	G1	G0	Gain (dB)
0	0	0	0	0	0
0	0	0	0	1	-1.5
0	0	0	1	0	-3
0	0	0	1	1	-4.5
0	0	1	0	0	-6
0	0	1	0	1	-15
0	0	1	1	0	-18
0	0	1	1	1	-21
0	1	0	0	0	-24
0	1	0	0	1	-27
0	1	0	1	0	-30
0	1	0	1	1	-33
0	1	1	0	0	-36
0	1	1	0	1	-39
0	1	1	1	0	-42
0	1	1	1	1	-45
1	0	0	0	0	-48
1	0	0	0	1	-51
1	0	0	1	0	-54
1	0	0	1	1	-57
1	0	1	0	0	-60
1	0	1	0	1	-63
1	0	1	1	0	-66
1	0	1	1	1	-69
1	1	0	0	0	-72
1	1	0	0	1	-75
1	1	0	1	0	-78
1	1	0	1	1	-81
1	1	1	0	0	-84
1	1	1	0	1	-87
1	1	1	1	0	-90
1	1	1	1	1	-93

6.3.4 DAC Register

G4	G3	G2	G1	G0	Gain (dB)
0	0	0	0	0	0
0	0	0	0	1	-3
0	0	0	1	0	-6
0	0	0	1	1	-9
0	0	1	0	0	-12
0	0	1	0	1	-15
0	0	1	1	0	-18
0	0	1	1	1	-21
0	1	0	0	0	-24
0	1	0	0	1	-27
0	1	0	1	0	-30
0	1	0	1	1	-33
0	1	1	0	0	-36
0	1	1	0	1	-39
0	1	1	1	0	-42
0	1	1	1	1	-45
1	0	0	0	0	-48
1	0	0	0	1	-51
1	0	0	1	0	-54
1	0	0	1	1	-57
1	0	1	0	0	-60
1	0	1	0	1	-63
1	0	1	1	0	-66
1	0	1	1	1	-69
1	1	0	0	0	-72
1	1	0	0	1	-75
1	1	0	1	0	-78
1	1	0	1	1	-81
1	1	1	0	0	-84
1	1	1	0	1	-87
1	1	1	1	0	-90
1	1	1	1	1	-93

7.0 Frequency Synthesizer

The Frequency Synthesizer (FS) block generates the CODEC sampling clock from a reference crystal oscillator of 14.316MHz. The output frequency of the FA is equal to 256 times fs (where fs = CODEC sampling frequency).

One of the 236 frequencies may be generated by the FS. The selection of the FS output frequency is done via the 8 FSEL lines, FSEL[7:0].

Table 7-1 gives the Frequency Selection, where the FSEL[7:0] address is given in decimal equivalent. FOUT-actual is the FS output frequency for a given FSEL code and %error gives the difference between the FOUT-actual and the target FOUT-spec.

Table entries in bold refer to the 14 critical sampling frequencies. The %error for these frequencies fall within ±0.15%.

Table 7-1 FS Output Frequencies

FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)
0	3909.064	27	4369.507	54	4955.795	81	5720.082
1	3924.890	28	4386.642	55	4971.528	82	5746.201
2	3938.710	29	4415.502	56	4993.722	83	5785.830
3	3947.978	30	4433.451	57	5019.331	84	5804.024
4	3951.554	31	4448.952	58	5049.208	85	5843.400
5	3957.289	32	4462.475	59	5084.517	86	5887.335
6	3994.978	33	4488.185	60	5115.520	87	5915.640
7	4030.968	34	4500.090	61	5126.888	88	5949.967
8	4033.391	35	4523.725	62	5151.419	89	5992.466
9	4047.543	36	4544.287	63	5178.675	90	6023.197
10	4067.614	37	4565.689	64	5202.762	91	6059.049
11	4084.752	38	4584.401	65	5243.408	92	6101.420
12	4092.416	39	4601.810	66	5268.739	93	6138.624
13	4112.477	40	4605.974	67	5290.646	94	6168.715
14	4131.170	41	4609.590	68	5326.637	95	6214.410
15	4142.940	42	4660.807	69	5346.220	96	6260.786
16	4164.977	43	4713.176	70	5377.855	97	6292.090
17	4178.655	44	4716.962	71	5412.550	98	6331.663
18	4209.761	45	4739.804	72	5437.608	99	6377.947
19	4221.108	46	4759.973	73	5456.555	100	6408.610
20	4237.097	47	4783.460	74	5493.094	101	6453.425
21	4255.520	48	4806.457	**75**	**5514.194**	102	6491.839
22	4276.976	49	4833.430	76	5519.377	103	6544.963
23	4302.284	50	4847.240	77	5523.920	104	6579.963
24	4302.284	51	4877.589	78	5592.969	**105**	**6615.339**
25	4327.892	52	4906.113	79	5668.549	106	6670.513
26	4350.087	53	4934.972	80	5680.359	107	6711.562

FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)
108	6750.135	140	8636.202	172	11910.952	204	19225.830
109	6802.259	141	8691.776	173	12046.394	205	19617.129
110	6848.533	142	8773.284	174	12189.804	206	20034.515
111	6895.441	143	8849.634	175	12356.559	207	20418.775
112	6935.281	144	8924.950	176	12494.930	208	20836.550
113	6991.211	145	9005.628	177	12663.325	209	21286.672
114	7049.961	146	9088.574	178	12817.220	210	21750.434
115	7089.679	147	9175.964	179	12983.677	**211**	**22049.203**
116	7139.960	148	9219.179	180	13159.926	212	22721.435
117	7190.960	149	9321.614	181	13332.077	213	23238.391
118	7250.145	150	9433.923	182	13511.104	214	23821.904
119	7295.177	151	9519.947	183	13697.066	215	24394.863
120	7359.169	**152**	**9599.872**	184	13866.865	216	24989.860
121	7402.459	153	9710.015	185	14099.921	217	25634.440
122	7457.292	154	9805.854	186	14286.387	218	26303.566
123	7512.943	155	9904.215	187	14487.810	**219**	**27446.976**
124	7573.812	156	10025.133	188	14703.165	220	27703.490
125	7626.775	157	10098.416	189	14914.583	221	28566.238
126	7690.332	158	10209.387	190	15147.624	222	29417.563
127	7752.630	159	10302.837	191	15380.664	223	30295.247
128	7813.706	160	10418.275	192	15627.413	224	31254.825
129	7877.421	161	10532.214	193	15871.938	**225**	**32007.953**
130	7935.969	162	10634.518	**194**	**16018.697**	**226**	**33080.364**
131	**7989.955**	163	10755.709	195	16379.408	227	34502.080
132	8066.782	164	10875.217	196	16665.917	228	35691.971
133	8129.315	165	10986.188	197	16948.390	229	37053.418
134	8196.592	**166**	**11028.389**	198	17244.987	**230**	**38003.505**
135	8262.340	167	11263.617	199	17537.275	231	40005.262
136	8329.953	168	11360.718	200	17839.642	232	41693.039
137	8389.453	169	11485.561	201	18177.148	**233**	**44098.407**
138	8474.195	170	11616.166	202	18511.939	234	45495.044
139	8544.813	171	11774.671	**203**	**18905.810**	**235**	**48006.315**

8.0 Electrical Specification

8.1 Absolute Maximum Ratings

Sym.	Description	Min	Max	Units
V_{DD}	Supply Voltage	-0.5	6.5	V
V_I	Input Voltage	-0.5	V_{DD} + 0.5	V
V_O	Output Voltage	-0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-40	125	°C
	Power Dissipation	TBD	TBD	V

8.2 Recommended DC Operating Conditions

Sym.	Description	Min	Max	Units
V_{DD}	Supply Voltage	4.5	5.5	V
A_{VD}	Supply Voltage	4.75	5.25	V
T_{OP}	Operating Temperature	0	70	°C

8.3 General Specification (V_{DD} = 5.0V)

Sym.	Description	Condition	Min	Typ.	Max	Units
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$	-10		+10	uA
I_{IH}	High Level Input Current	$V_{IN} = V_{DD}$	-10		+10	uA
I_{OZ}	Tri-State Output Leakage Current	$V_{OUT} = 0/V_{DD}$	-10		+10	uA
V-	Schmitt Negative Threshold	TTL-STATIC CMOS-STATIC	0.8 1.5		1.3 2.5	V
V+	Schmitt Positive Threshold	TTL-STATIC CMOS-STATIC	1.4 2.5		2.1 3.5	V
V_H	Schmitt Hysteresis	TTL-STATIC CMOS-static		0.6 1.0		V
V_{IL}	low Level Input Voltage	TTL-STATIC			0.8	V
V_{IH}	High Level Input Voltage	TTL-STATIC	2.0			V
V_{OL}	Low Level Output Voltage	TTL-STATIC			0.4	V
V_{OH}	High Level Output Voltage	TTL-STATIC	2.4			V
R_{PD}	Pull-Down Resistance	$V_{IN} = V_{DD}$	50		200	KΩ
R_{PU}	Pull-Up Resistance	$V_{IN} = V_{SS}$	50		200	KΩ
C_{IN}	Input Capacitance	FREQ = 1MHz @ 0V			5	pF
C_{OUT}	Output Capacitance	FREQ = 1MHz @ 0V			5	pF
C_{IO}	Bi-Directional Capacitance	FREQ = 1MHz @ 0V			5	pF
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V		2	25	mA
I_{KLU}	I/O Latch-Up Current	$V < V_{SS}$, $V > V_{DD}$	100			mA
V_{ESD}	Electrostatic Protection	C = 100pF, R = 1.5KΩ	2000			V

8.4 Timing Parameters

8.4.1 AT Bus Timing

Description	Sym	Min	Max	Units
OSC (14.318 MHz) Frequency	t_{OSCP}	14.000	14.500	MHz
OSC High Width	t_{OSCH}	32	40	ns
OSC Low Width	t_{OSCL}	32	40	ns
SYSCLK Frequency	t_{SCKP}	8	9	MHz
SYSCLK High Width	t_{SCKH}	50	70	ns
SYSCLK Low Width	t_{SCKL}	55	70	ns
RESET to RST#	t_{RST}	40	80	ns
IOR#/IOW# Command Width	t_{CMDW}	120		ns
Write Data Setup to IOW# Rising	t_{WDSU}	30		ns
Write Data Hold from IOW# Rising	t_{WDHD}	15		ns
Read Access Time	t_{RAC}	20	50	ns
Address Setup to IOR#/IOW# Falling	t_{ASU}	50		ns
Address Hold from IOR#/IOW# Rising	t_{AHD}	30		ns
DACK# Setup to IOR#/IOW# Falling	t_{DKSU}	40		ns
DACK# Hold from IOR#/IOW# Rising	t_{DKHD}	160		ns
SD Hold from IOR# Rising	t_{DHR}	0	20	ns
DRQ Hold from IOR#/IOW# Falling	t_{DRHD}	0	25	ns

8.4.2 CD ROM/FM/Game Port Interface Timing

Description	Sym	Min	Max	Units
SA to CA Delay	t_{CA}	3	20	ns
SA to XCS#/FMCSn/MIXCS#	t_{XCS}	5	20	ns
SD to CD/XD Delay	t_{XD}	5	30	ns
CD/XD to SD Delay	t_{XSD}	5	30	ns
CD/XD Read Data Hold	t_{XDH}	5		ns
IOR#/IOW# to XIOR#/XIOW# Delay IOR#/IOW# to GPR#/GPW# Delay	t_{CMDD}	3	20	ns
IOW# to CD/XD Enable Delay	t_{XDE}	5	20	ns
XDRQ to DRQ# Delay	t_{DRQ}	5	20	ns
DACK# to XDAK# Delay	t_{XDAK}	5	20	ns

8.5 DC Electrical Characteristics

Description	Sym	Min	Max	Units	Conditions
Operating Supply Voltage	Vcc	4.5	5.5	V	
High Level Input Voltage	V_{IH}	2.4	Vcc + 0.3	V	Vcc = min
High Level Input Voltage for RESET	V_{IHa}	3.5	Vcc + 0.3	V	Vcc = min
Low Level Input Voltage	V_{IL}	-0.3	0.8	V	Vcc = max
High Level Output Voltage	V_{OH}	Vcc-0.5	Vcc	V	Ioh = -4mA Vcc = max
Low Level Output Voltage	V_{OL}		0.2	V	Iol = 4MA Vcc = min
Input Leakage Current	I_{IL}		10	uA	Vcc = max
Input Leakage Current with 5K pull-up resistor	I_{ILa}	-100	-500	uA	Vin = 0V
Input Leakage Current with 50K pull-up resistor	I_{ILb}	-10	-50	uA	Vin = 0V
Output Leakage Current	I_{OL}		10	uA	Vcc = max
Static or Power-down Mode Current	I_{PD}		300	uA	Vcc = max

8.6 Absolute Maximum Ratings

Description	Sym	Min	Max	Units	Conditions
Supply Voltage	Vcc	-0.3	7.0	V	
Storage Temperature	Ts	-65	+125	C	
Ambient Operating Temperature	Ta	-45	+85	C	

8.7 Pin Specifications - Analog

(@ V_{DD} = 5.0V, 25°C)

Pin Name	Parameter	Test Condition	Min	Typ.	Max	Units
Inputs						
MICR MICL LINER LINEL CDR CDL AUXR AUXL CINR CINL	Signal bandwidth Input range	Sine Wave	10 0.5	- -	20K 3.0	Hz Volts
Outputs						
OUTR OUTL	Signal bandwidth Output range	Sine Wave Load = 10KΩ, 25pF	10 0.5	- -	20K 3.0	Hz Volts
MIXOUTR MIXOUTL	Signal Bandwidth Output Range	Sine Wave	10		20K	Hz

Pin Name	Parameter	Test Condition	Min	Typ.	Max	Units
VREFI		DC		1.75		Volts
VREF		DC		2.5		Volts

8.8 Volume Setting

Parameter	Test Conditions	Min	Typ.	Max	Units
Input Gain/Atten. Range:	Input @ 1Hz, 2.5Vpp wrt ACOM				
16 levels (MIC, LINE, CD, AUX)		-33		12	dB
16 levels (ADC)		0		22.5	dB
32 levels (DAC)		-93		0	dB
32 levels (LOUT)		-46.5		0	dB
Step Size:					
16 levels (MIC, LINE, CD, AUX)		2.6	3.0	3.4	dB
16 levels (ADC)		1.3	1.5	1.7	dB
32 levels (DAC)	90 to -81dB)	2.6	3.0	3.4	dB
	(-84 to -93dB)	2.0	3.0	4.0	dB
32 levels (LOUT)		1.3	1.5	1.7	dB
Mute Level			-80		dB
SNR			-80		dB
THD			0.04		%
Total Dynamic Range			80		dB
Interchannel Isolation			60		dB
Interchannel Gain Mismatch		-0.5		+0.5	dB
Gain Drift			100		ppm/°C

8.9 Timing Characteristics

Figure 8-1 Register/CD/FM/Mixer/Sound Port I/O Read Cycle

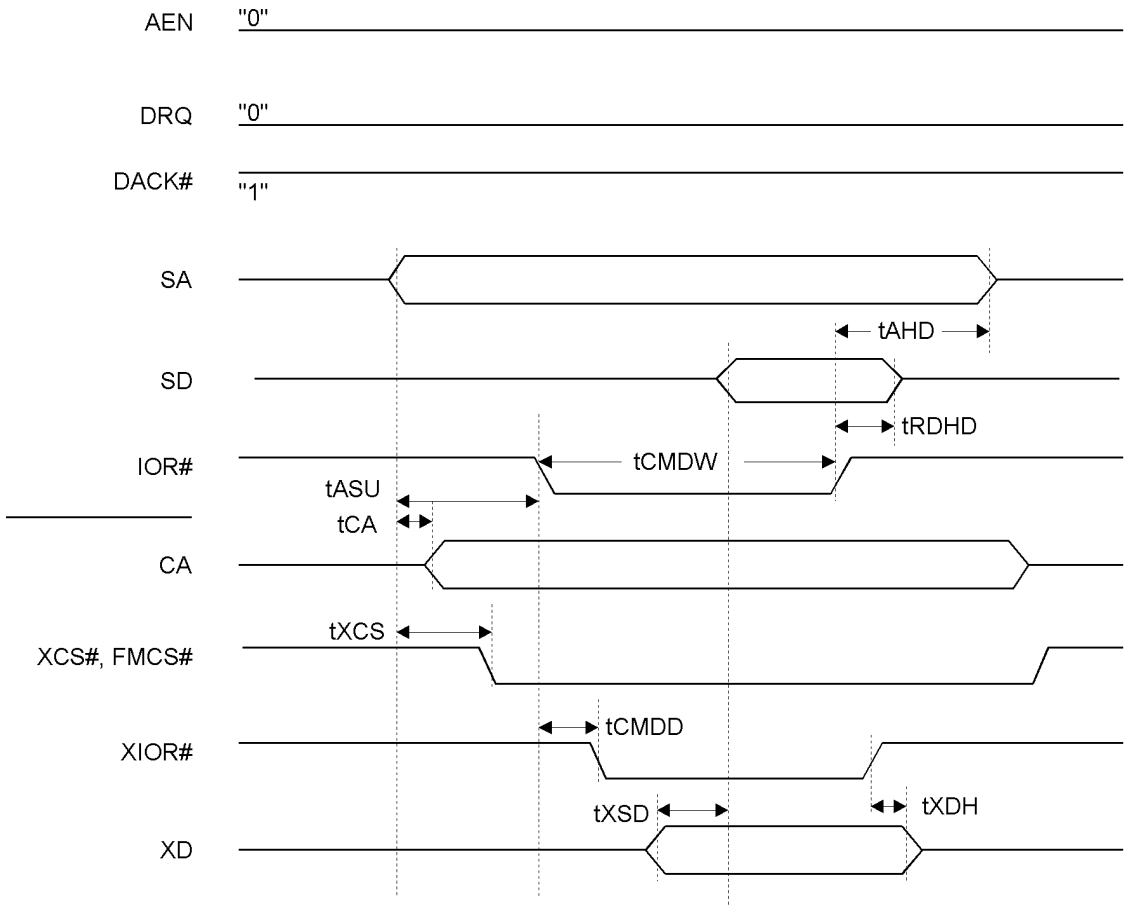


Figure 8-2 DMA Write/Playback Cycle

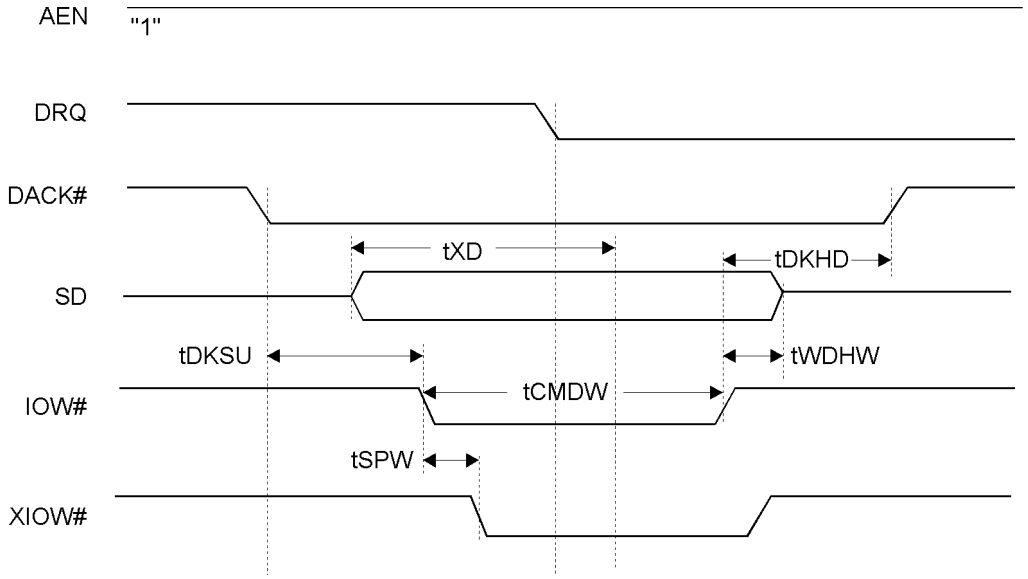


Figure 8-3 DMA Read/Capture Cycle

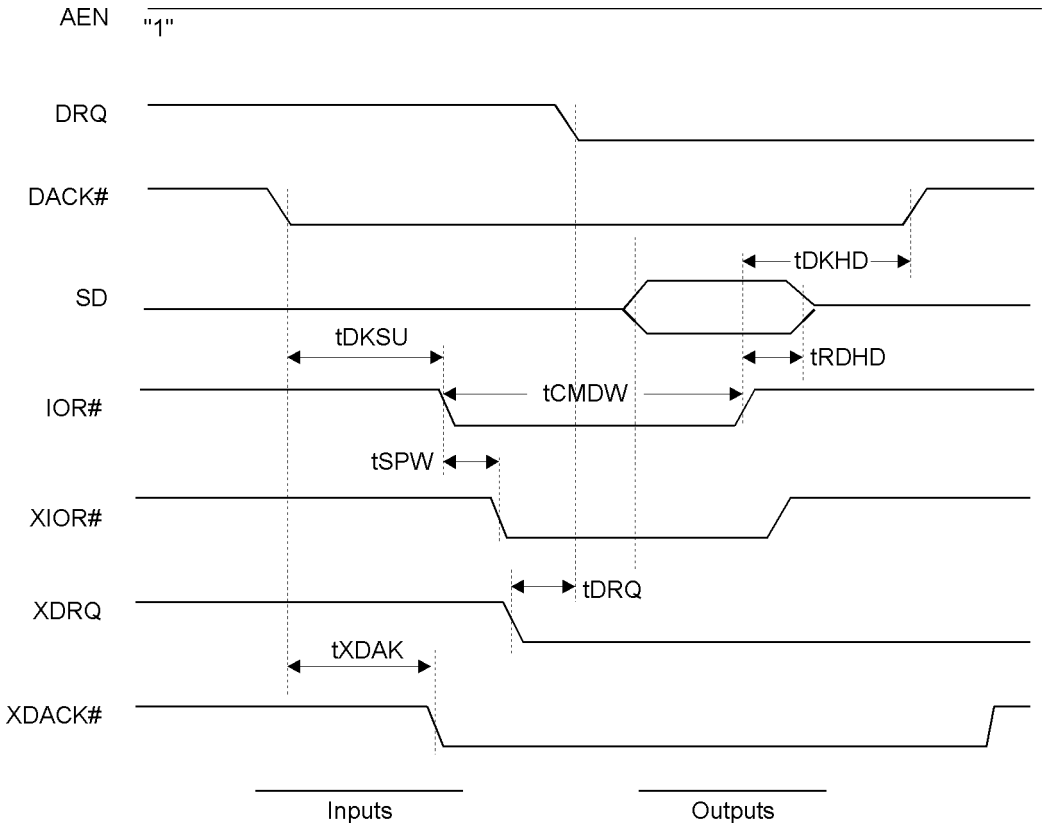
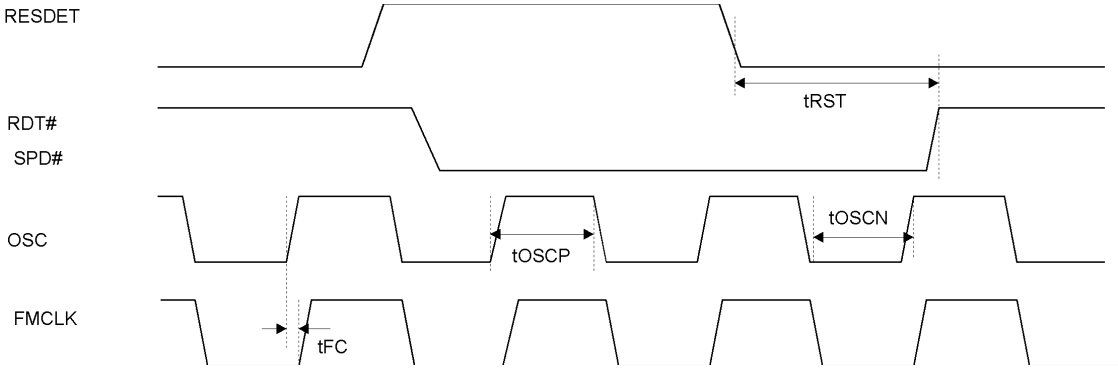
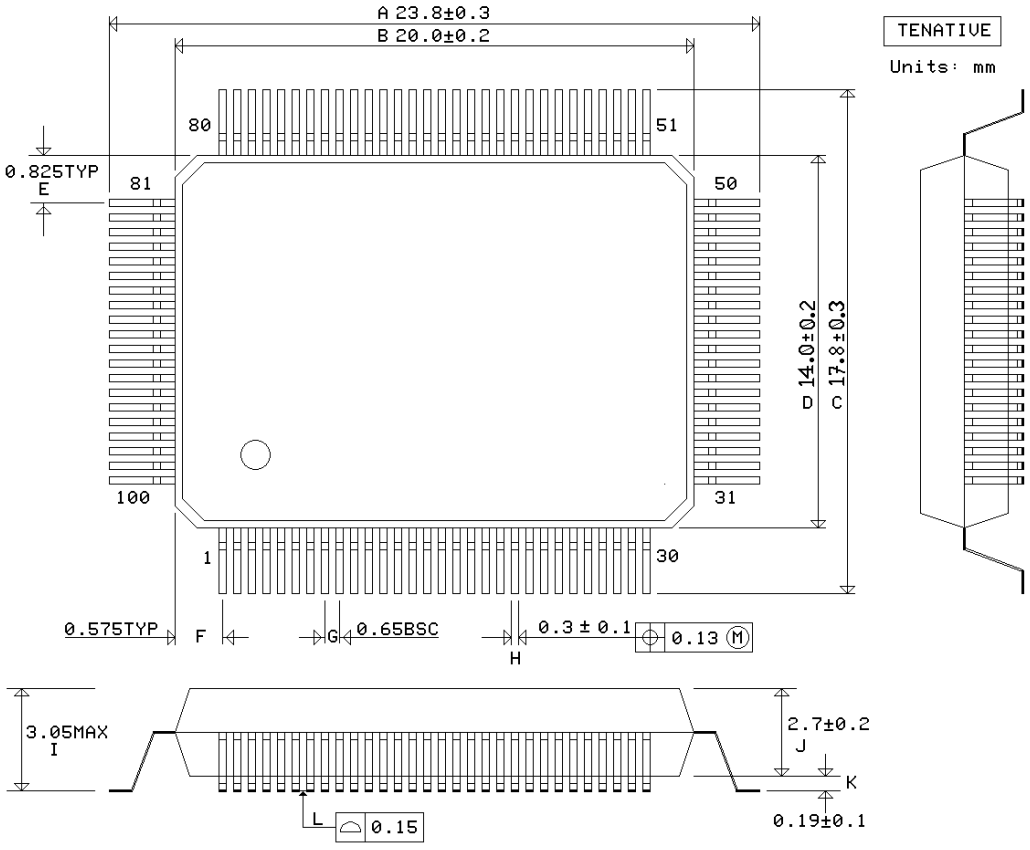
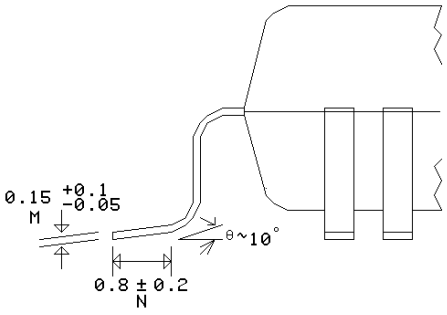


Figure 8-4 RESET and CLK Timing



9.0 Mechanical Package





DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	23.5	24.1	.925"	.949"	Maximum Width LEAD TO LEAD
B	19.8	20.2	.779"	.795"	Maximum Width PACKAGE ENVELOPE
C	17.5	18.1	.689"	.713"	Maximum Height LEAD TO LEAD
D	13.8	14.2	.543"	.559"	Maximum Height PACKAGE ENVELOPE
E	0.825 TYP		.0325" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	0.575 TYP		.0226" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	3.05	——	.120"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	2.5	2.9	.098"	.114"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.09	0.29	.0035"	.0114"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.15	——	.006"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.010"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT